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EXAMINER

B3M1/0226

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ART UNIT

PAPER NUMBER

18

2309  
DATE MAILED:

02/26/96

This is a communication from the examiner in charge of your application.  
COMMISSIONER OF PATENTS AND TRADEMARKS

This application has been examined

Responsive to communication filed on 1/4/95

This action is made final.

A shortened statutory period for response to this action is set to expire THREE month(s), ZERO days from the date of this letter.  
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

**Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:**

1.  Notice of References Cited by Examiner, PTO-892.
2.  Notice of Draftsman's Patent Drawing Review, PTO-948.
3.  Notice of Art Cited by Applicant, PTO-1449.
4.  Notice of Informal Patent Application, PTO-152.
5.  Information on How to Effect Drawing Changes, PTO-1474.
6.

**Part II SUMMARY OF ACTION**

1.  Claims 1-23 are pending in the application.

Of the above, claims \_\_\_\_\_ are withdrawn from consideration.

2.  Claims \_\_\_\_\_ have been cancelled.

3.  Claims \_\_\_\_\_ are allowed.

4.  Claims 1-23 are rejected.

5.  Claims \_\_\_\_\_ are objected to.

6.  Claims \_\_\_\_\_ are subject to restriction or election requirement.

7.  This application has been filed with informal drawings under 37 C.F.R. 1.85 which are acceptable for examination purposes.

8.  Formal drawings are required in response to this Office action.

9.  The corrected or substitute drawings have been received on \_\_\_\_\_. Under 37 C.F.R. 1.84 these drawings are  acceptable;  not acceptable (see explanation or Notice of Draftsman's Patent Drawing Review, PTO-948).

10.  The proposed additional or substitute sheet(s) of drawings, filed on \_\_\_\_\_, has (have) been  approved by the examiner;  disapproved by the examiner (see explanation).

11.  The proposed drawing correction, filed \_\_\_\_\_, has been  approved;  disapproved (see explanation).

12.  Acknowledgement is made of the claim for priority under 35 U.S.C. 119. The certified copy has  been received  not been received  been filed in parent application, serial no. \_\_\_\_\_; filed on \_\_\_\_\_.

13.  Since this application appears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.

14.  Other

**EXAMINER'S ACTION**

Art Unit: 2309

1. The following is a quotation of the first paragraph of 35 U.S.C. § 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

The specification is objected to under 35 U.S.C. § 112, first paragraph, as failing to adequately teach how to make and/or use the invention, i.e. failing to provide an enabling disclosure.

The disclosure presents an invention as shown in figure 1 and specification at page 9, lines 21 and 22, where "the voltage vcc is used to power the solid state memory 13 and is also input to the power director 29". However, Applicant claims "without varying a voltage being supplied to elements of said electronic system other than said memory integrated circuit". The specification and drawings fail to disclose that there is no variable voltage supplied to the elements of the electronic system.

2. Claims 1-20 and 22 are rejected under 35 U.S.C. § 112, first paragraph, for the reasons set forth in the objection to the specification.

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --  
(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on

Art Unit: 2309

sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-23 are rejected under 35 U.S.C. § 102(b) as being clearly anticipated by Dias et al, U.S. Pat. No. 4977537.

As per claim 1, Dias discloses supplying a variable voltage to said memory integrated circuit (abstract, figure 5 and column 2, lines 11-14) and generating address and control signals (column 14, lines 14-22 and figure 5).

As per claim 21, Dias discloses supplying a variable voltage to said memory integrated circuit (abstract, figure 5 and column 2, lines 11-14) and supplying different voltages during different periods (figure 5, abstract and column 14, lines 14-22).

As per claim 23, Dias discloses supplying a variable voltage to said memory integrated circuit (abstract, figure 5 and column 2, lines 11-14) and generating address and control signals (column 44, lines 14-22 and figure 5).

Claims 2-20 and 22 are also taught by Dias's reference.

4. (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1-23 are rejected under 35 U.S.C. § 102(e) as being clearly anticipated by Fung, U.S. Pat. No. 5396635.

As per claim 1, Fung discloses supplying a variable voltage to said memory integrated circuit (abstract, last three lines and figure

1, devices 9, 15, 13 and 11) and generating address and control signals (column 4, lines 51-64 and figure 1).

As per claim 21, Fung discloses supplying a variable voltage to said memory integrated circuit (abstract, last three lines and figure 1, devices 9, 15, 13 and 11) and supplying different voltages during different periods (abstract and figure 1).

As per claim 23, Fung discloses supplying a variable voltage to said memory integrated circuit (abstract, last three lines and figure 1, devices 9, 15, 13 and 11) and generating address and control signals (column 4, lines 51-64 and figure 1).

Claims 2-20 and 22 are also taught by Fung's reference.

5. Applicant's arguments with respect to claims 1-23 have been considered but are deemed to be moot in view of the new grounds of rejection.

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to George Davis whose telephone number is (703) 305-9640.

G. Davis

February 22, 1996

  
GEORGE B. DAVIS  
PRIMARY PATENT EXAMINER  
GROUP 2300